

REMARKS

Claims 18, 19, 36, 41-43, 54-64, 70-77, 79-85, 87-91 and 95-103 are pending. Applicants propose amendment of claims 18, 36, 42, 43, 54, 58, 63, 64, 79, 87, 88, 91, 97-100 and 102. It is respectfully submitted that entry of the amendments after final rejection places the application in condition for allowance. Attached hereto is marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned **“Version with markings to show changes made.”**

On page 2 of the Office Action, the Examiner has noted that the prior response did not address some informalities in regard to claims 97, 98 and 100. The present amendment corrects these informalities.

Claims 58, 63, 64, 97, 98 and 100 were rejected under 35 USC §112, second paragraph, as being indefinite. In regard to claims 58, 63 and 64, these claims have been amended to correct the lack of antecedent basis for “the semiconductor element.” Furthermore, the above amendments to claims 97-100 address the remaining informalities noted by the Examiner. It is respectfully submitted that the amended claims overcome the rejection.

Claims 18, 19, 36, 42, 43, 57-64, 71, 87-91 and 97-101 were rejected under 35 USC §102(e) as being anticipated by Kata et al. Favorable reconsideration of this rejection is earnestly solicited in view of the proposed amendments made herein.

Claims 18, 36, 42, 43, 87, 88, 90 and 91 have been amended to more clearly describe the invention. It should be noted that an internal part corresponds to, for example, a circuit formed on a semiconductor element, and an external part corresponds to, for example, an external circuit. The claims further specify that lead lines are provided which connect the protruding electrodes and pads formed on a semiconductor element. The lead lines are located between the semiconductor element and the resin layer.

The Examiner considers adhesive layer 43 illustrated in Figs. 8 and 9 of Kata et al. to correspond to the claimed resin layer. If so, lead lines must be located between the adhesive layer 43 and the semiconductor chip (element). However, Kata et al. teaches a structure in which the wiring layer 62 is located above the resin layer 42 but is not located between the semiconductor chip and the resin layer 42. The above structure does not have a satisfactory resistance to an invasion of water. Taking this into consideration, Kata et al. teaches the use of a coating film 46 (column 8, lines 36-45). After the coating film 46 is provided, it is necessary to remove portions thereof attached to the bumps 67.

In contrast thereto, the claimed invention provides lead lines located between the resin layer and the semiconductor element. Thus, there is no need to take into consideration an invasion of water. As such, it is possible to prevent an invasion of water without using a coating film as taught by Kata et al. Furthermore, the present invention does not need the step of removing the unwanted portions of the coating film.

Claim 41 was rejected under 35 USC §103(a) as being unpatentable over Kata et al. Favorable reconsideration of this rejection is earnestly solicited.

Claims 41 depends from claim 18. It is respectfully submitted that claim 18 is patentable over Kata et al. for the reasons discussed above.

Claims 54-56 were rejected under 35 USC §102(e) as being anticipated by Kitahara. This rejection is respectfully traversed in view of the amendments made herein.

Kitahara teaches a portion corresponding to a base which is located on the upper surface side of the chip. However, Kitahara fails to teach or suggest that the semiconductor element is placed in a cavity formed in a flexible base. Accordingly, claims 54-56 distinguish over Kitahara.

Claims 79 and 81-83 were rejected under 35 USC §102(b) as being anticipated by McMahon. Favorable reconsideration of this rejection is respectfully requested.

McMahon teaches a wiring layer which extends from an electrode on the chip along a front, a side and a back surface thereof, and is connected to an external electrode.

In contrast thereto, proposed amended claim 79 defines that the protruding electrodes on the semiconductor element pass through wiring pattern through holes and can be connected to external electrodes. This structure does not need extending of the wiring layer along the surfaces of the chip.

Claims 88 and 97-100 were rejected under 35 USC §102(e) as being anticipated by White. Furthermore, claim 102 was rejected under 35 USC §103(a) as being unpatentable over White further in combination with Cole. Favorable reconsideration of these rejections is earnestly solicited.

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The Examiner argues that White discloses a compressed resin layer 3, 36. Element 33 of White is a dielectric layer and element 36 is a second dielectric layer.

As noted above, claim 88 has been amended to further characterize the invention. It is respectfully submitted that the cited art fails to teach or suggest the features of the amended claims.

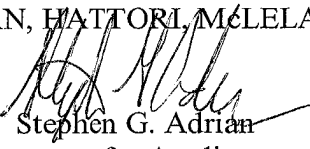
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI, MCLELAND & NAUGHTON, LLP


Stephen G. Adrian
Attorney for Applicants
Reg. No. 32,878

Attachment: Version with marking to show changes made

Attorney Docket No. 980233
Suite 1000, 1725 K Street
Washington, D.C. 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
SGA/arf

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IN THE CLAIMS:

Please amend claims 18, 36, 42, 43, 54, 58, 63, 64, 79, 87, 88, 91, 97-100 and 102 as follows:

18. (Three Times Amended) A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; [and]

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and

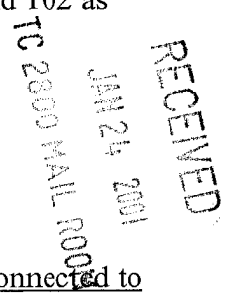
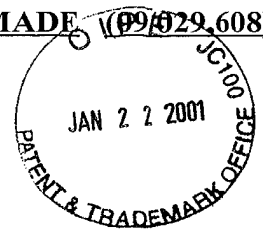
a [compressed] resin layer which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes;

wherein the lead lines are located between the semiconductor element and the resin layer.

36. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and external connection electrodes are provided which are to be electrically connected to external terminals; [and]

lead lines each connecting one of the electrode pads and one of the external



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connecting electrodes so that the external connecting electrodes and the internal part are connected through the lead lines; and

a resin layer provided on the surface of the semiconductor element so as to cover the external connection electrodes,

wherein the external connection electrodes are exposed at a lateral surface of the resin layer and the lead lines are located between the semiconductor element and the resin layer.

42. (Three Times Amended) A semiconductor device comprising:

a semiconductor element having [protruding electrodes formed on] a surface [thereof] on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed;

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and

a first [compressed] resin layer that is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and

a second [compressed] resin layer provided so as to cover at least a back surface of the semiconductor element;

wherein the lead lines are located between the semiconductor element and the resin layers.

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43. (Three Times Amended) A semiconductor device comprising:

a semiconductor element having [protruding electrodes formed on] a surface [thereof] on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed;

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines;

a [compressed] resin layer which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and

external connection protruding electrodes provided to the ends of the protruding electrodes exposed from the resin layer;

wherein the lead lines are located between the semiconductor element and the resin layer.

54. (Twice Amended) A semiconductor device comprising:

a semiconductor element;

protruding electrodes functioning as external connection terminals;

a wiring board having a flexible base on which leads are formed, the leads having ends connected to the semiconductor element and other ends connected to the protruding electrodes and the flexible base having a cavity in which the semiconductor element is placed;
and

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a sealing resin sealing the semiconductor element,

wherein there are provided extending portions that are formed to the wiring board so that the extending portions laterally extend from a position in which the semiconductor element is placed, the protruding electrodes being formed on the extending portions.

58. (Twice Amended) The semiconductor device as claimed in claim 57, wherein the semiconductor [element or] elements are connected to the electrode plate in a flip-chip bonding formation.

63. (Three Times Amended) The semiconductor device as claimed in claim 57, wherein the semiconductor [element or] elements are partially exposed from the sealing resin.

64. (Three Times Amended) The semiconductor device as claimed in claim 57, further comprising a heat radiating member in a position close to the semiconductor [element or] elements.

79. (Twice Amended) A semiconductor device comprising:
a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a compressed resin layer which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes;

an interposer to which the semiconductor device main body is attached, the

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interposer being attached to a side of the protruding electrodes of the semiconductor main body,
a wiring pattern to which the semiconductor device main body is connected being formed on a
base member of the interposer;

an adhesive which is provided between the semiconductor device main body and
the interposer and which bonds the semiconductor device main body to the interposer;

a conductive member which electrically connects the semiconductor device main
body and the interposer; and

external connection terminals which are connected to wiring pattern through holes
formed in the base member and are arranged on a surface of the semiconductor device main body
opposite to the surface on which the protruding electrodes are provided.

87. (Twice Amended) A semiconductor wafer on which semiconductor elements are
provided, comprising:

a semiconductor wafer including a plurality of semiconductor elements having a
surface on which electrode pads connected to an internal part of the semiconductor elements and
protruding electrodes to be connected to an external part are formed; [and]

lead lines each connecting one of the electrode pads and one of the protruding
electrodes so that the protruding electrodes and the internal part are connected through the lead
lines; and

a [compressed] resin layer which is formed on the surface of the semiconductor
elements and seals at least a lateral surface of the protruding electrodes;

wherein the lead lines are located between the semiconductor elements and the

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resin layer.

88. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; [and]

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and

a [compressed] resin layer which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes,

wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer, and the lead lines are located between the semiconductor element and the resin layer.

91. (Twice Amended) A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; [and]

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and

a resin layer which is formed on the surface on the semiconductor element and seals a lateral surface and a top of the protruding electrodes, the resin layer slightly covering upper

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portions of the protruding electrodes;

wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer and the lead lines are located between the semiconductor element and the resin layer.

97. (Twice Amended) The semiconductor device as claimed in claim 88, wherein the [compressed] resin layer is formed by disposing a film between the protruding electrodes and a mold, which thus contacts the [sealing] resin layer through the film.

98. (Twice Amended) The semiconductor device as claimed in claim 88, wherein a sheet-shaped resin is used as the [sealing] resin layer.

99. (Twice Amended) The semiconductor device as claimed in claim 88, wherein a reinforcement plate is loaded onto a mold before the substrate is loaded onto the mold in forming the [compressed] resin layer.

100. (Twice Amended) The semiconductor device as claimed in claim 88, wherein: a film used in forming the [compressed] resin layer is formed of an elastically deformable substance, and [the] ends of the protruding electrodes are caused to fall in the film when the resin layer is formed by using a mold; and

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the film is detached from the resin layer when the protruding [electrode is]
electrodes are exposed so that the ends of the protruding electrodes can be exposed from the resin
layer.

102. (Twice Amended) The semiconductor device as claimed in claim 88, wherein the
[compressed] resin layer comprises a plurality of sealing resins having different characteristics.